Abstract of the Disclosure

A semiconductor integrated circuit device provided with a SRAM realizing low power consumption and high speed is to be provided. Out of memory circuits which cause a timing generator circuit which selects writable and readable memory cells with the address selector circuit, conveys write signals to a memory cell selected by a write circuit, conveys read signals from a memory cell selected by a read circuit, and receives a clock signal, to generate operational timing signals to be conveyed to an address selector circuit, a write circuit and a read circuit, a circuit in which the operational timing is not too tight is configured of a higher threshold voltage MOSFET than the MOSFETs of other circuits.